Notice of References Cited	Application/Control No. 09/763,204	Applicant(s)/Patent Under Reexamination CLERMIDY ET AL.	
	Examiner Yolanda Wilson	Art Unit 2184	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,646,989 b1	11-2003	Khotimsky et al.	370/238
	B	US-5,065,308	11-1991	Evans, Richard A.	714/11
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chean et al. A Taxonomy of Reconfiguration Techniques for Fault-Tolerant Processor Arrays. IEEE Computer, pages 55-69.
	V	Roychowdhury et al. Efficient Algorithms for Reconfiguration in VLSI/WSI Arrays. IEEE Transactions, vol. 39, no. 4. pages 480 489.
	W	Belkhale et al. Reconfiguration Strategies for VLSI Processor Arrays and Trees Using a Modified Diogenes Approach. IEEE Transactions, vol. 41, no. 1. pages 83-96.
	X	Kung et al. Fault-Tolerant Array Processors Using Single-Track Switches. IEEE Transactions, vol. 38, no. 4. pages 501-514.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/763,204	Applicant(s)/Patent Under Reexamination CLERMIDY ET AL.	
	Examiner Yolanda Wilson	Art Unit 2184	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chen et al. A Comprehensive Reconfiguration Scheme for Fault-Tolerant VLSI/WSI Array Processors. IEEE Transactions, vol. 46, no 12. pages 1363-1371.
	V	Varvarigou et al. Reconfiguring Processor Arrays Using Multiple-Track Models: The 3-Track-1-Spare-Approach. IEEE Transactions, vol. 42, no. 11. pages 1281-1293.
	W	Ku et al. Structural Fault Tolerance in VLSI-Based Systems. IEEE. pages 50-55.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.